DAC348x EVM

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1 Introduction

1.1 Overview

This document is intended to serve as a basic user's guide for the DAC3484/2 EVM Revision F, and DAC34H84/SH84 EVM revision C and above.

The Texas Instruments DAC348x evaluation module (EVM) is a family of circuit boards that allows designers to evaluate the performance of Texas Instruments' DAC348x family of digital-to-analog converters (DAC). The 16-bit, ultra low power family of DACs has either 16-bit wide or 32-bit wide DDR LVDS data input, integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO, on-chip PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC348x under a variety of clock, data input, and IF output conditions.

	DAC3484	DAC3482	DAC34H84	DAC34SH84
Output Channel	4	2	4	4
EVM Part No.	DAC348x Rev. F	DAC348x Rev. F	DAC34H84 Rev. C	DAC34H84 Rev. C
Maximum DAC Rate	1.25GSPS	1.25GSPS	1.25GSPS	1.5GSPS
Digital Interface	16-bit LVDS Interface	16-bit LVDS Interface	32-bit LVDS Interface	32-bit LVDS Interface
Maximum Data Rate per Channel	312.5MSPS	625MSPS	625MSPS	750MSPS
Maximum LVDS Bus Toggle Rate	1.25GSPS	1.25GSPS	1.25GSPS	1.5GSPS
Pattern Generator Support	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100 with limited data rate support

For ease of use as a complete IF transmit solution, the DAC348xEVM includes the Texas Instruments CDCE62005 clock generator/jitter cleaner for clocking the DAC348x. Besides providing a high-quality, low jitter DAC sampling clock to the DAC348x, the CDCE62005 also provides FPGA clocks to the TSW1400EVM (or TSW3100EVM) as FPGA reference clocks.

The EVM can be used along with Texas Instruments TSW1400 or TSW3100 with limited data rate support (up to 1.25GSPS LVDS Bus rate) to perform a wide varieties of test and measurements. The TSW1400 generates the test patterns that are fed to the DAC348x through a maximum 1.5 GSPS LVDS Bus port. These EVM boards are also compatible with Altera® and Xilinx® FPGA development platforms for rapid evaluation and prototyping. The on-board HSMC connector input allows direct connection to the HSMC compatible Altera development platforms, and the externally attached FMC-DAC-Adapter board available from TI enables the connection of the EVM to the Xilinx development platforms with FMC headers.

For evaluation of complete RF transmit solution, see the TSW308x EVM. The EVM integrates the DAC348x, TRF3705, and LMK04800 devices into one RF transmitter system.

See the TSW308x EVM web folders at:

http://www.ti.com/tool/tsw3085evm
http://www.ti.com/tool/tsw3084evm
http://www.ti.com/tool/tsw30h84evm
http://www.ti.com/tool/tsw30sh84evm

1.2 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW1400 or TSW3100 used for pattern generation.

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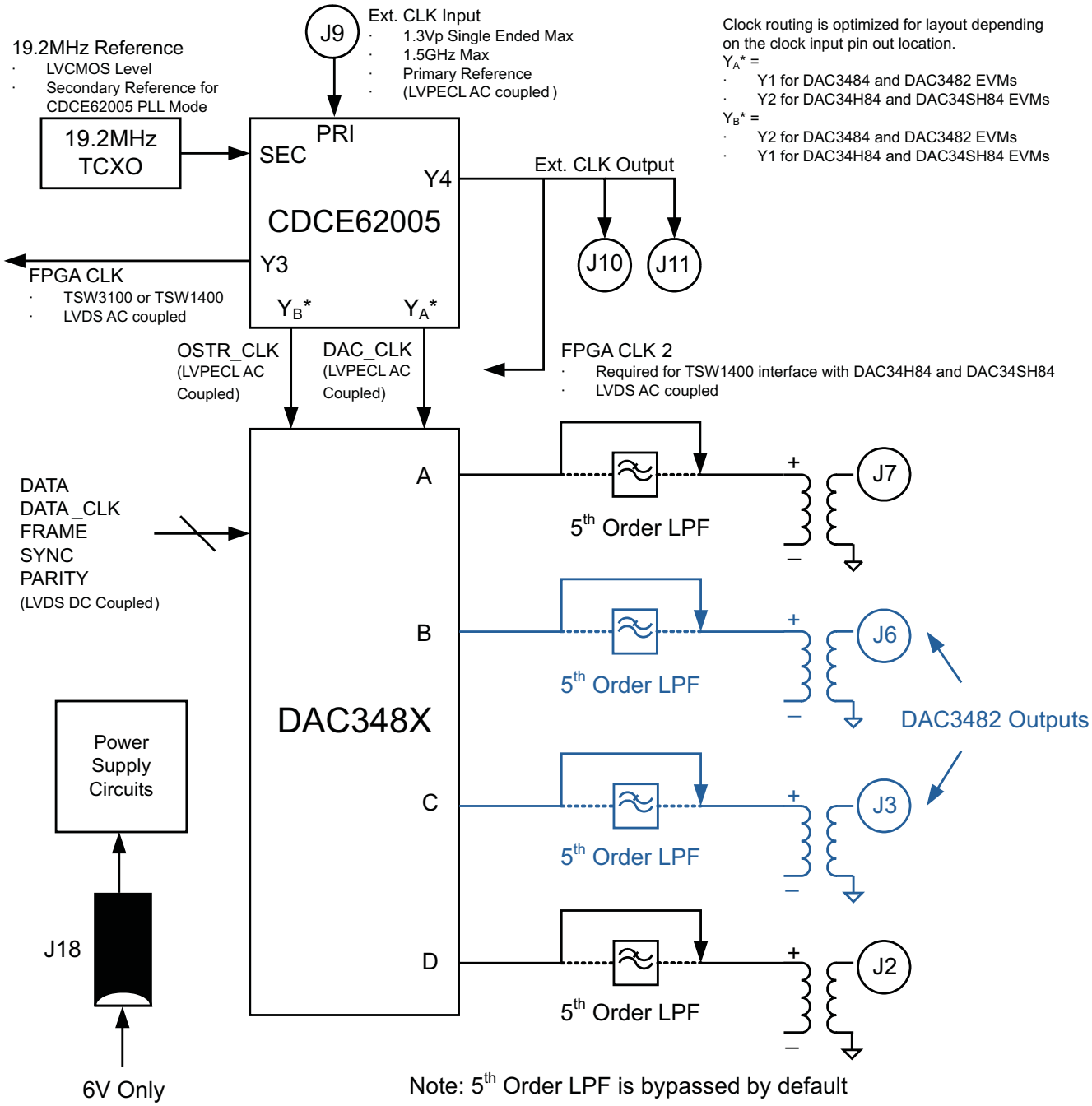

Figure 1. DAC348x EVM Block Diagram

2 Software Control

2.1 Installation Instructions

- Open folder named DAC348x_Installer_vxpx (xpx represents the latest version)
- Run Setup.exe
- Follow the on-screen instructions
- Once installed, launch the program by clicking on the DAC348x_GUI_vxpx program in Start>Texas Instruments DACs. The installation directory is located at C:\Program Files\Texas

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Instruments\DAC348x

- When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
  - When a pop-up screen opens, select “Continue Downloading”.
  - Follow the on screen instructions to install the USB drivers
  - If needed, you can access the drivers directly in the install directory

2.2 Software Operation

The software allows programming control of the DAC device and the CDC device. The front panel provides a tab for full programming of each device. The GUI tabs provide more convenient and simplified interface to the most used registers of each device.

Each device, including the DAC3484, DAC3482, and DAC34H84/SH84, has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC348x and the last for the CDCE62005.

2.2.1 Input Control Options

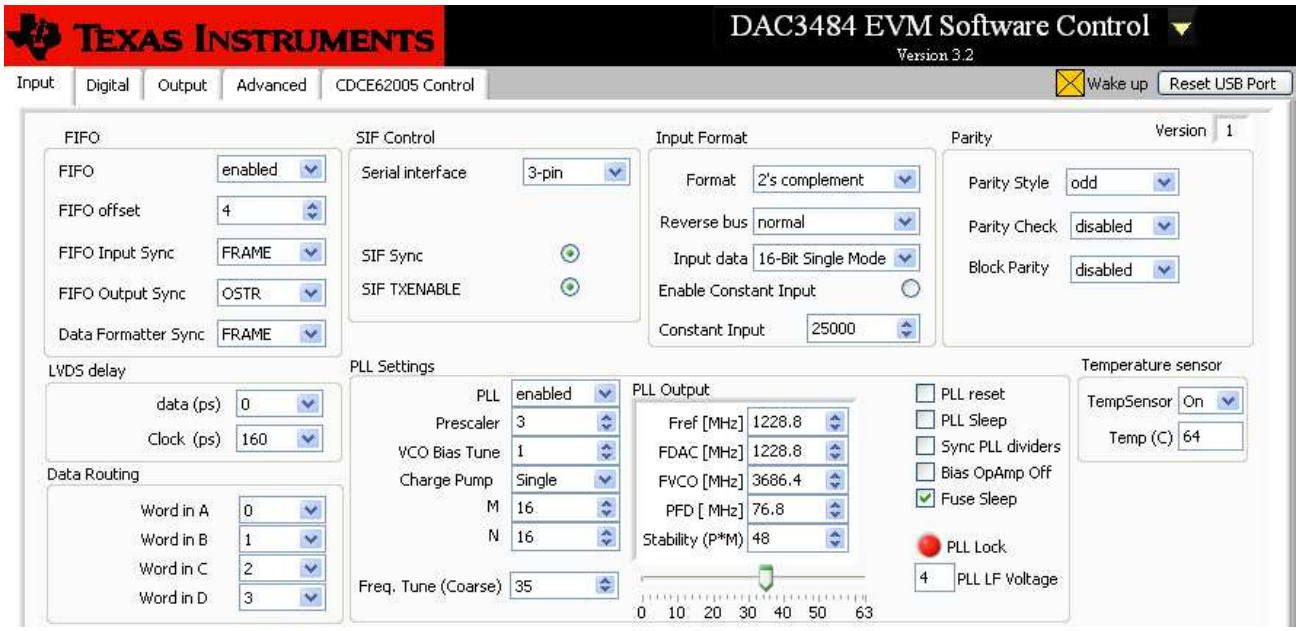

Figure 2. Input Control Option

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path.
  Note: the DAC3482 does not support this mode
- SIF Control: provides control of the Serial Interface (3-wires or 4-wires) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (i.e., 2s complement or offset binary)
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC3484/2 die temperature.

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2.2.1.1 FIFO Settings

The DAC348x has 8-samples deep FIFO to relax the timing requirement of a typical transmitter system. The FIFO has an input pointer and an output pointer, and both pointers can accept various input sources as reset triggers of input and output pointer position. One important application for input and output pointer control is the ability to synchronize multiple DACs in the system. For additional information, see the relevant DAC348x data sheet.

- FIFO Offset: The default position of FIFO output pointer after reset by the synchronization source. This setting can be used to change the latency of the DAC348x.
- Data Formatter Sync (DAC3482 and DAC3484): Synchronization source for FIFO data formatter. Select between LVDS FRAME or LVDS SYNC signals.
- FIFO Sync Select (DAC34H84 and DAC34SH84): Select the internal digital routing of LVDS ISTR or LVDS SYNC to the FIFO ISTR path
- FIFO Input Sync: Synchronization source for FIFO input pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC to reset the FIFO input pointer position.
- FIFO Output Sync: Synchronization source for FIFO output pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, SPI register SIF-SYNC, and/or OSTR signal to reset the FIFO output pointer position.
  - For single device application without the need for precise latency control, Single Sync Source Mode may be used. The FIFO output pointer position can be reset with LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC. See the Single Sync Source Mode in the relevant DAC348x data sheet for details.
  - For multiple device synchronization, select the OSTR signal as the FIFO output synchronization source. If the DAC is configured to accept external DAC Clock input, then the OSTR signal is the external LVPECL signal to the OSTRP/N pins. If the DAC is configured to accept the internal on-chip PLL clock, then the OSTR signal is the internally generated PFD frequency. See the Dual Sync Sources Mode in the relevant DAC348x data sheet for details.

2.2.1.2 LVDS Delay Settings

Depending on the signal source implementation (i.e. TSW1400, TSW3100, or FPGA System), the following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:

- Set the on-chip LVDS DATA or DATACLOCK delay: The DAC348x includes on-chip LVDS DATA or DATACLK delay. The delay ranges from 0ps to 280ps with an approximate 40ps step. This LVDS DATACLOCK delay does not account for additional PCB trace-to-trace delay variation, only the internal DATACLK delay.
  - The TSW1400 pattern generator sends out LVDS DATA and DATACLK as center aligned signal. Additional DATACLK delay is not needed.
  - The TSW3100 pattern generator sends out LVDS DATA and DATACLK as edge-aligned signal. Typical setting of 160ps or more will help meet the timing requirement for most of the TSW3100 + DAC348x EVM setup.
- Modify the external LVDS DATACLK PCB trace delay: Additional trace length on the bottom side of the PCB can be added to the LVDS DATACLK PCB trace length. Set SJP9, SJP10, SJP11, and SJP12 to 2-3 position for approximately 220ps of trace delay.

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2.2.1.3 PLL Settings

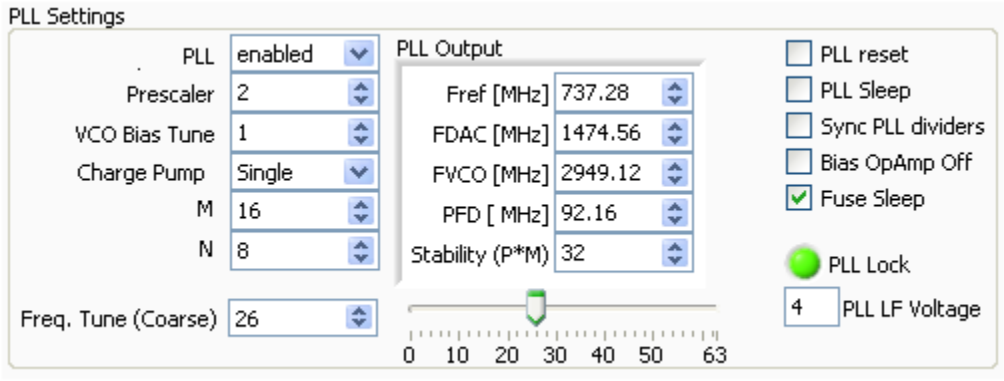

Figure 3. PLL Configuration

Follow the steps below to configure the PLL.

1. Enable PLL
2. Uncheck *PLL reset* and *PLL sleep*
3. Set *M* and *N* ratio such that F_{DAC} = (M)/(N) x Fref
4. For the DAC3482, DAC3484, and DAC34H84: Set the *prescaler* such that the F_{DAC} x prescaler is within 3.3GHz and 4GHz.
5. For the DAC34SH84, Set the *prescaler* such that the F_{DAC} x prescaler is within 2.7GHz and 3.3GHz.
6. Set *VCO Bias Tune* to “1”
7. *Charge Pump* setting

   (a) If stability (P x M) is less than 120, then set to “Single”.

   (b) If stability (P x M) is greater than 120, then set to “Double” or install external loop filter
8. Adjust the *Freq. Tune* (*coarse tune*) accordingly. For additional information, see the relevant DAC348x data sheet.

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2.2.2 Digital Block Options

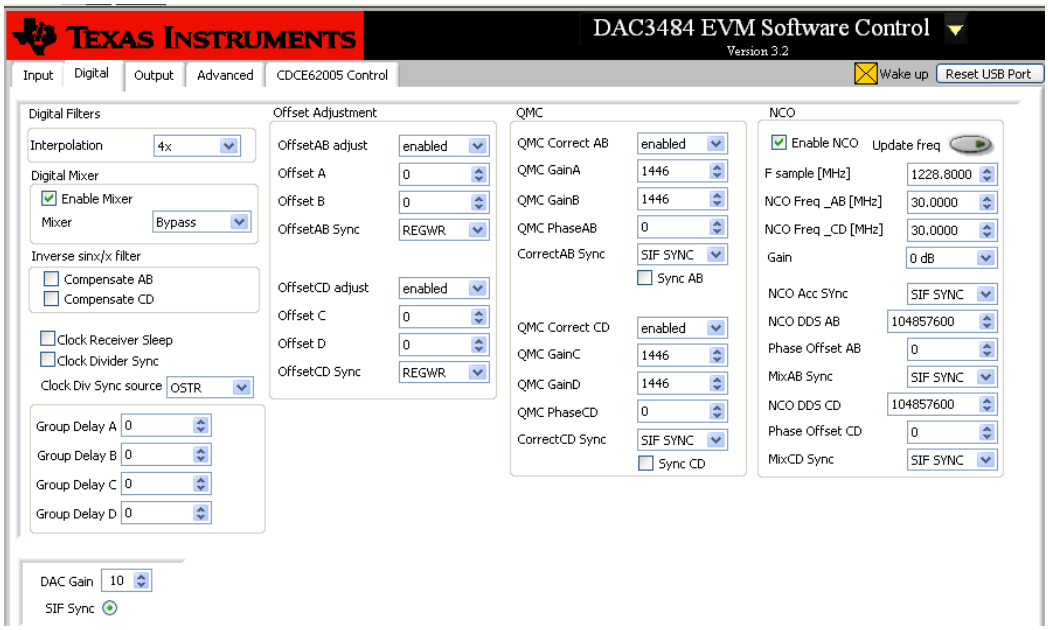

Figure 4. Digital Block Options

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (i.e. data rate x interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the "Enable Mixer" button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronization of the internal divided-down clocks using either FRAME, SYNC, or OSTR signal. Enable the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression. **Note:** This feature is not available for the DAC34SH84.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feed-through of the modulator output. This section requires syncing for proper operation. The synchronization options are listed below:
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x08 (offset A) or 0x0A (offset B) registers last.**
  - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source
  - SYNC: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x10 (QMC phase AB) or 0x11 (QMC phase CD) registers last.**

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  - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - SYNC: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency are listed below:
  1. Enter the DAC sampling frequency in *Fsample.*
  2. Enter the desired mixing frequency in both *NCO freq_AB* and *NCO freq_CD*.
  3. Press *Update freq*
  4. Sync the NCO block from the following options:
     - **REGWR: auto-sync from SIF register write. Writing to either Phase OffsetAB or Phase OffsetCD can create a sync event.**
     - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source. Refer to the datasheet for OSTR period requirement.
     - *SYNC*: sync from the external SYNC signal
     - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

2.2.3 Output Control Options

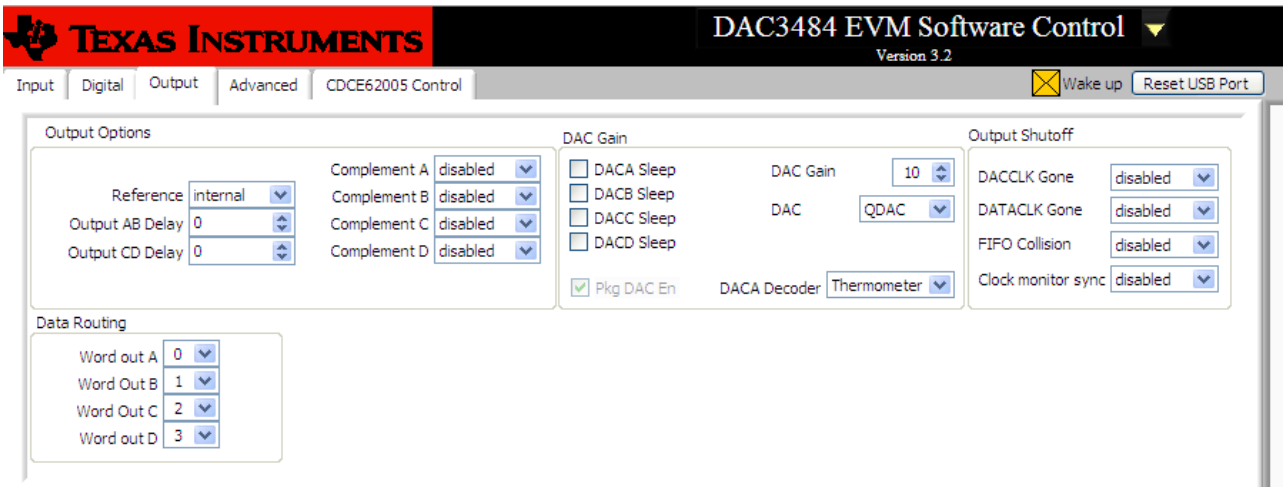

Figure 5. Output control Options

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note:** The DAC3482 does not support this mode.
- DAC Gain: configures the full-scale DAC current and DAC3484/DAC3482 mode. With Rbiaj resistor set at 1.28kΩ:
  - DAC Gain = 15 for 30mA full-scale current.
  - DAC Gain = 10 for 20mA full-scale current (default).
- Output Shutoff On: allows outputs to shut-off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

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2.2.4 CDCE62005

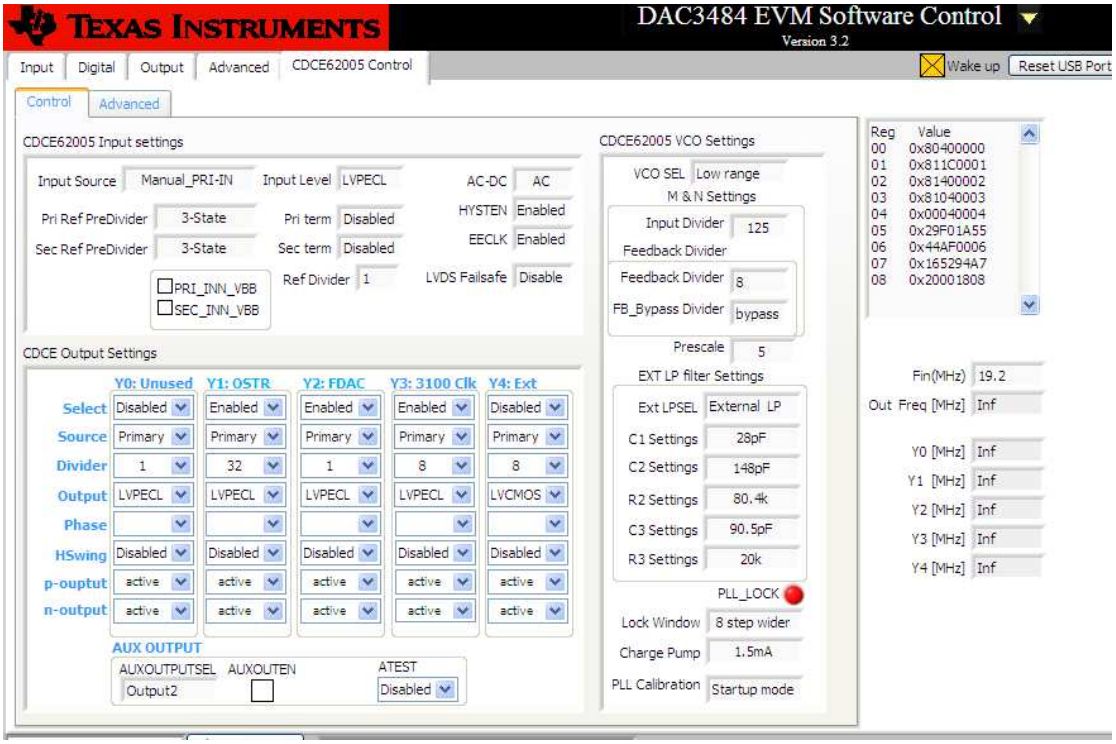

Figure 6. CDCE62005 Tab Configured for 4x Interpolation

Clock frequency control is determined by register values in the CDCE62005 Control tab. See the CDCE62005 data sheet for detailed explanations of the register configuration to change the clock frequency.

The following CDCE62005 outputs are critical to proper operation of the DAC348x:

- **Y_A*: DAC348x DAC sampling clock.** This clock is an ac coupled LVPECL. If the DAC348x is configured for internal PLL mode, this will be the reference clock input for the PLL block.
  - Y_A* = Y1 for DAC3484 and DAC3482 EVMs
  - Y_A* = Y2 for DAC34H84 and DAC34SH84 EVMs
- **Y_B*: DAC348x FIFO OSTR clock.** This clock is an ac coupled LVPECL. The clock rate for this should be at least F_{DAC}/*Interpolation/8*. See the DAC348x data sheet for more details.
  - The whole OSTR clock equation needs to take account of both the Y1 CDCE62005 clock divider ratio and the additional CDCP1803 divide-by-2 clock divider.
  - This OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - **Note:** The FIFO OSTR clock should be disabled when the DAC348x is configured in PLL mode.
  - Y_B* = Y2 for DAC3484 and DAC3482 EVMs
  - Y_B* = Y1 for DAC34H84 and DAC34SH84 EVMs
- **Y3: FPGA Clock 1.** This clock is an ac coupled LVDS. The clock rate for this should be
  - F_{DAC}/*interpolation/2* for DAC3484
  - F_{DAC}/*interpolation/4* for DAC3482, DAC34H84, and DAC34SH84
- **Y4: FPGA Clock 2.** This clock is an ac coupled LVDS. This clock must be enabled when using the DAC34H84 and DAC34SH84 with the TSW1400. The clock rate for this should be F_{DAC}/*interpolation/4* for DAC34H84, and DAC34SH84

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2.2.5 Register Control

- **Send All:** Sends the register configuration to all devices
- **Read All:** Reads register configuration from DAC348x device
- **Load Regs:** Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory: C:\Programs Files\Texas Instruments\DAC348x\EVM Configuration File Released.
  - Select *Load Regs* button.
  - Double click on the *EVM Configuration File Released* folder and respective sub-folders for the EVM.
  - Double click on the desired register file.
  - Click on *Send All* to ensure all of the values are loaded properly.
- **Save Regs:** Saves the register configuration for all devices

2.2.6 Miscellaneous Settings

- **Reset USB:** Toggle this button if the USB port is not responding. This generates a new USB handle address
  - **Note:** It is recommended that the board be reset after every power cycle and the “reset usb” button on the GUI be clicked.

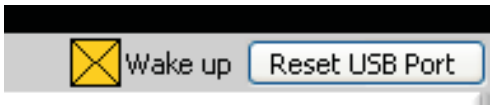

Figure 7. USB Port Reset

- **Exit:** Stops the program

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3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM with the TSW1400.

3.1 TSW1400 Overview

The TSW1400 is a high speed data capture and pattern generator board. When functioning as a pattern generator, it has a maximum LVDS bus rate of 1.5 GSPS, and this allows evaluation of the DAC348x with maximum 750 MSPS of input data rate per channel.

See the TSW1400 user's guide (SLWU079) for more detailed explanation of the TSW1400 setup and operation. This document assumes that the High Speed Data Converter Pro software (SLWC107) is installed and functioning properly.

3.2 Test Block Diagram for TSW1400

The test set-up for general testing of the DAC348x with the TSW1400 pattern generation card is shown in Figure 8.

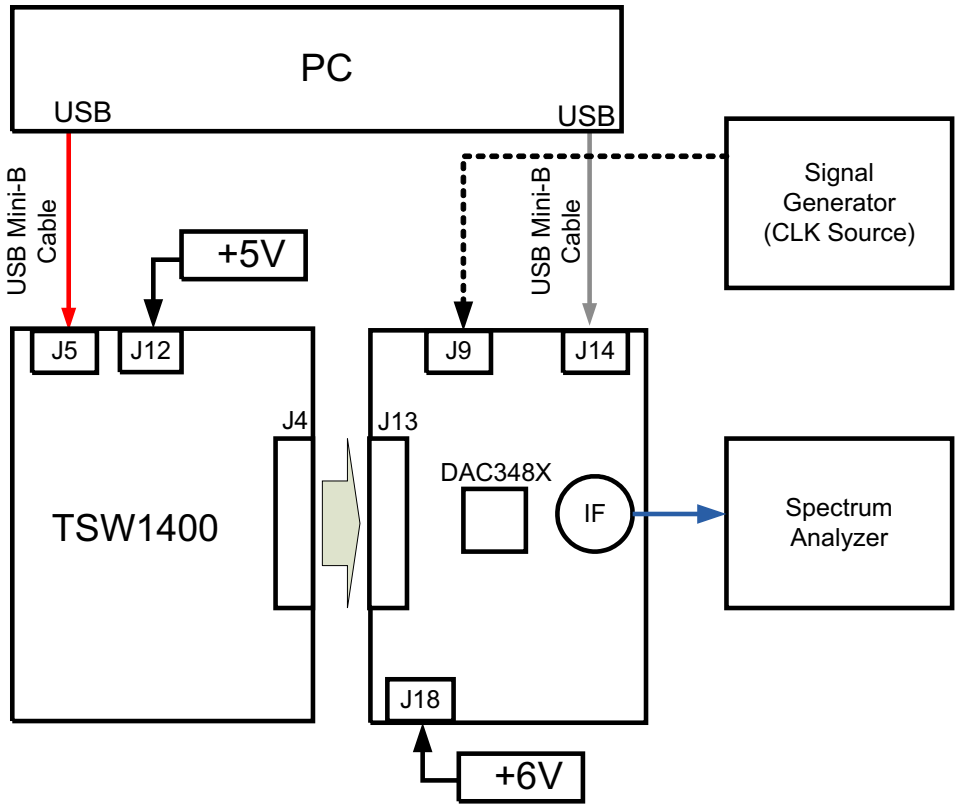

Figure 8. Test Set-up Block Diagram for TSW1400

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3.3 Test Setup Connection

TSW1400 Pattern Generator.

1. Connect 5 V power supply to J12, *5V_IN* jack of the TSW1400 EVM.
2. Connect PC's USB port to J5 USB port of the TSW1400 EVM. The cable should be a standard A to mini-B connector cable.

DAC348xEVM

1. Connect J13 connector of DAC348xEVM to J4 connector of TSW1400 EVM.
2. Connect 6V to the J18, *Power In* jack of the DAC3484 EVM.
3. Connect PC's USB port to J14 USB port of the DAC348x EVM. The cable should be a standard A to mini-B connector cable.
4. Provide a 1.3Vp, 1.5GHz max clock at J9, *CLKIN* SMA port of DAC348x EVM.
5. Connect the IF output port of J2, J3, J6, or J7 to the spectrum analyzer.

Table 1. DAC348xEVM Jumpers: (make sure the following jumpers are at their default setting)

Reference Designator	Setting	Function
JP2	1-2	DAC348x TXENABLE.
JP3	2-3	DAC348x SLEEP.
JP4	2-3	CDCE62005 Primary Input LVPECL Bias Enable.
JP5	1-2	CDCE62005 Reference Input Select.
JP6	1-2	CDCE62005 Power Down.
JP7	short	19.2MHz TCXO Enable.
JP8, JP9, JP12, JP13	short	SPI connection break point. This allows routing of SPI connection to external system if troubleshooting is needed.
JP10	1-2	6V Input Select. Default is 6V at J18.
JP11	open	For DAC34H84/SH84 EVM only. Allows SPI and IO logic threshold to switch among 1.8V, 2.5V, or 3.3V.
SJP9, SJP10, SJP11, SJP12	1-2	DAC348x DATACLK delay. Default is zero trace delay.

3.4 DAC348x Example Setup Procedure

1. Provide the clock input **1228.8** MHz at 1.5Vrms at J9 SMA Connector of the DAC348x EVM.
2. Turn on power to the board and press the reset SW1 button on the EVM
3. Press the "Reset USB Port" button in GUI and verify USB communication.
4. Select the appropriate EVM platform on the software menu.

Figure 9. EVM Platform Selection

5. Click "LOAD REGS", browse to the installation folder and load example file "*DAC3484_FDAC_1228p8MHz_4xint_NCO_30MHz_QMCon.txt*". This file contains settings for 4x interpolation with the DAC3484 running at 1228.8MSPS. Load this file and wait a couple of seconds for the settings to go into effect. The DAC3482, DAC34H84, and DAC34SH84 equivalent example files are also available in the installation folder.

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3.5 TSW1400 Example Setup Procedure

1. Start the High Speed Converter Pro GUI program. When the program starts, select the DAC tab and then select the corresponding device in the “Select DAC” menu.

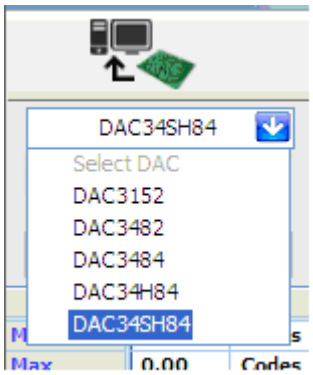

Figure 10. Select DAC348x Devices in the High Speed Converter Pro GUI Program

2. When prompted *Load DAC Firmware?*, select *YES*.

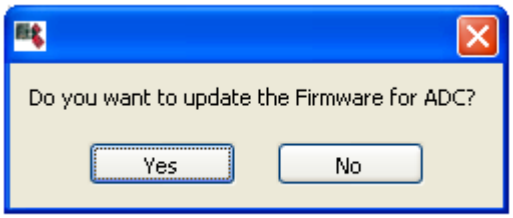

Figure 11. Load DAC Firmware Prompt

3. Click on the button labeled “Load File to transfer into TSW 1400”, located near the top left of the GUI.

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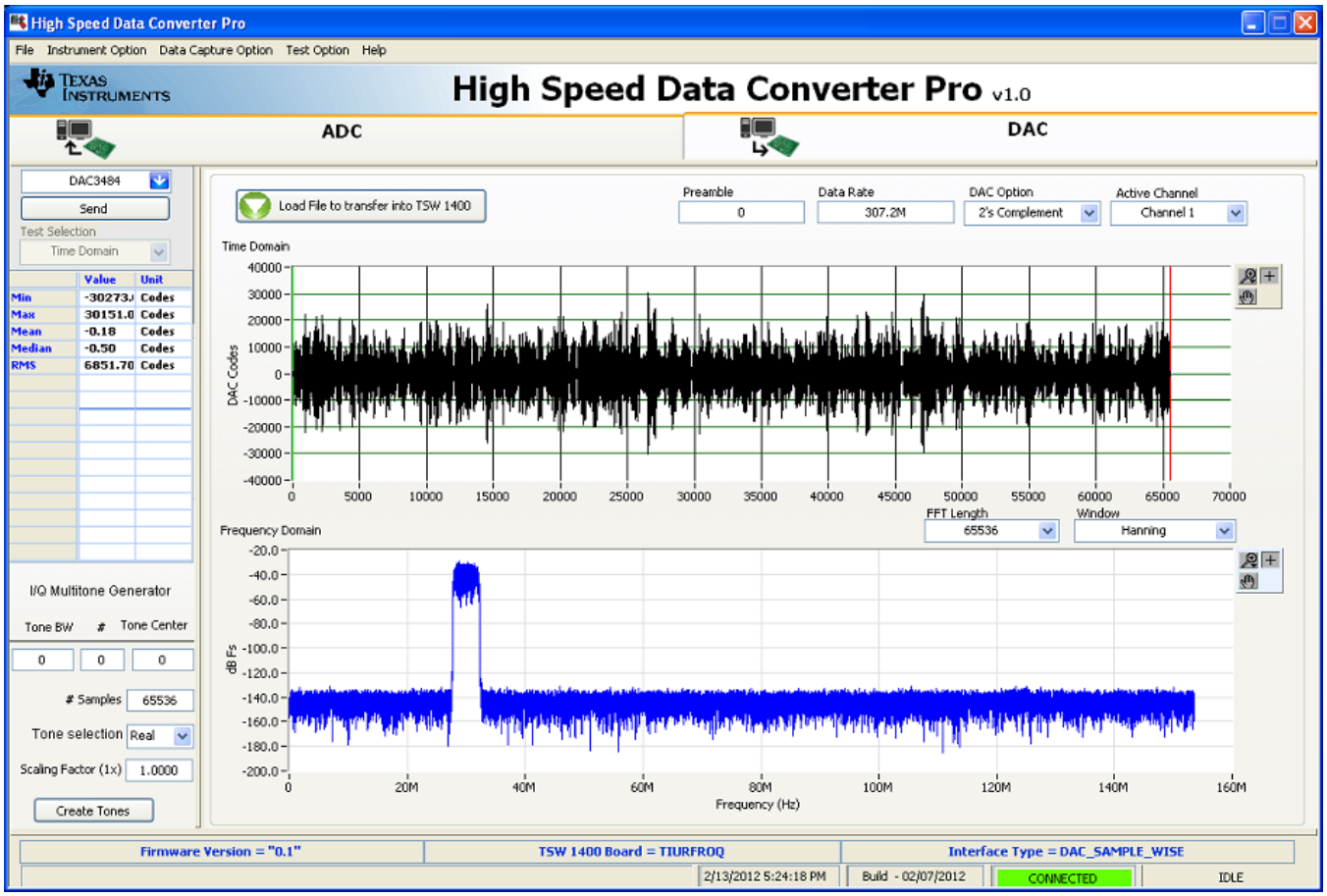

Figure 12. Load File to Transfer into TSW1400

4. Select the file "WCDMA_TM1_complexIF30MHz_Fdata307.2MHz_1000.tsw" under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles. The data rate of the file selected will depend on the sampling rate and interpolation ratio of the DAC configuration.
5. Enter 307.2M for the "Data Rate" and 2's complement for the "DAC Option".
6. Select Hanning for "Window".
7. In the “DAC Selection” panel on the left side of the GUI, click on “Send” to load the data into memory.
8. **Toggle the SIF SYNC button of the DAC348x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**
9. Verify the spectrum using the Spectrum Analyzer at the four IF outputs of the DAC348x EVM (J7, J6, J3, and J2).
   - For the DAC3482 EVM, the IF outputs are at the J6 and J3 SMA connector
10. The expect results are shown in Figure 13 (NCO enabled at 30MHz) and Figure 14 (NCO disabled).

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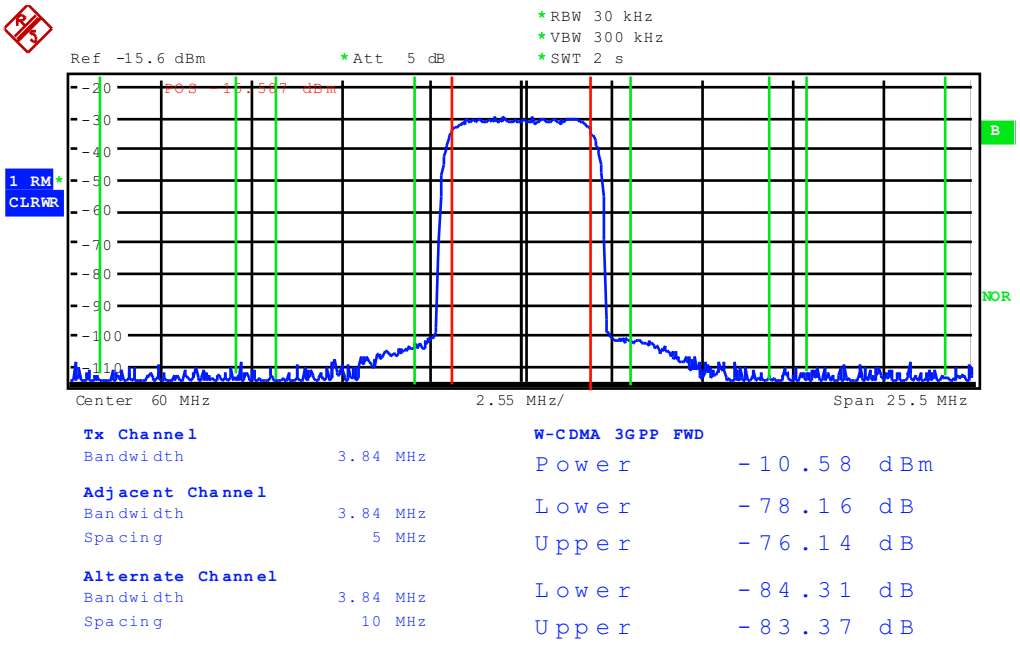
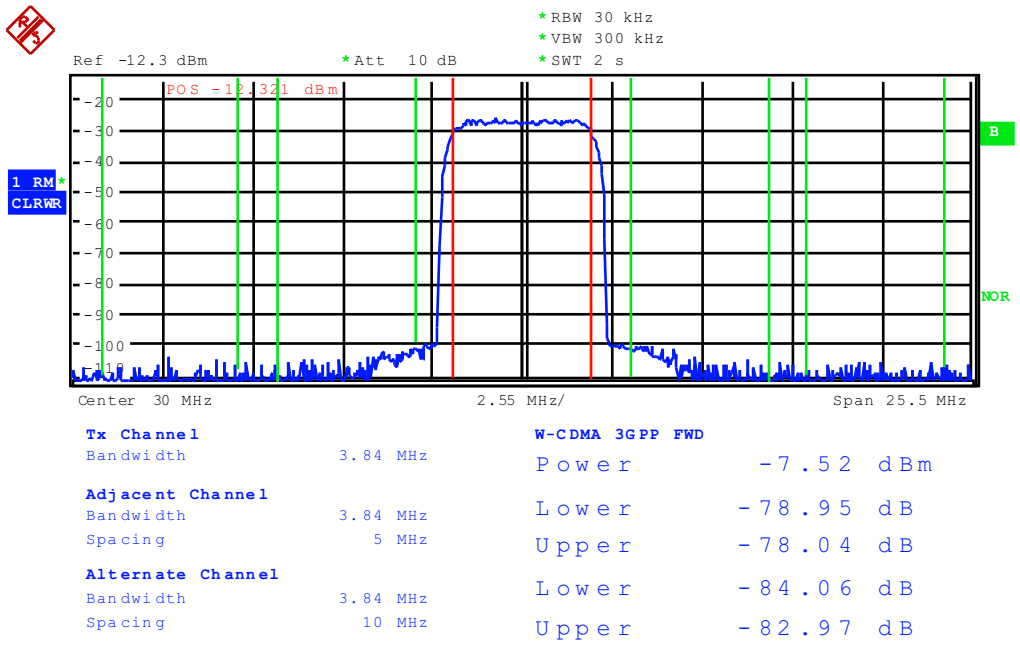


(baseband = 30MHz, NCO = 30MHz with NCO Gain disabled, QMC Gain = 1446)

Figure 13. DAC348x Transformer Coupled Output at 60MHz IF



(baseband = 30MHz, NCO disabled, QMC Gain = 1024)

Figure 14. DAC348x Transformer Coupled Output at 30MHz IF

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4 Basic Test Procedure with TSW3100

This section outlines the basic test procedure for testing the EVM with TSW3100.

4.1 TSW3100 Overview

The TSW3100 is a high speed pattern generator board. The LVDS Bus rate is limited to 1.25GSPS, and this limits the maximum input data rate per channel of DAC34SH84 to 625MSPS. To evaluate the DAC34SH84 at 1.5GSPS DAC sampling rate, 4x or higher interpolation filter must be enabled. To evaluate the DAC34SH84 at 1.5GSPS DAC sampling rate with 2x interpolation filter (i.e. 750MSPS of input data rate per channel), the TSW1400 must be used.

See the TSW3100 user's guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. The TSW30SH84 needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

The DAC348xEVM sends the FPGA reference clock to the FPGA of the TSW3100EVM in LVDS format. Therefore, a 100-Ω LVDS termination resistor is needed at the TSW3100 FPGA clock input. All the latest TSW3100EVMs from TI have the 100-Ω termination installed at the bottom side of the board on pins T31 and T32 of the FPGA. Contact TI Application Support if the 100-Ω termination is missing and assistance is needed for the 100-Ω installation.

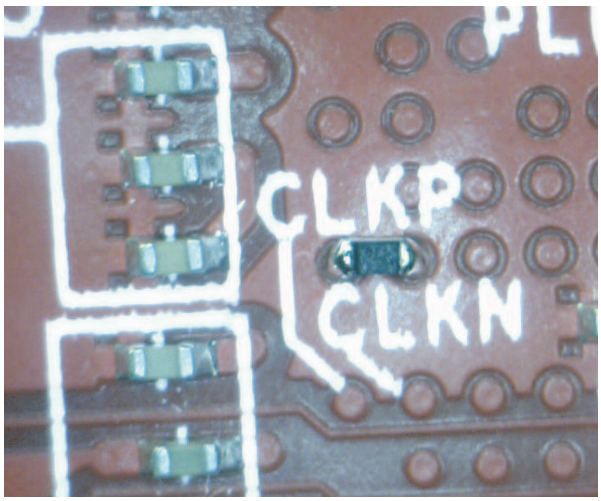

Figure 15. TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA

4.2 Test Block Diagram for TSW3100

The test set-up for general testing of the DAC348x with the TSW3100 pattern generation card is shown in Figure 16.

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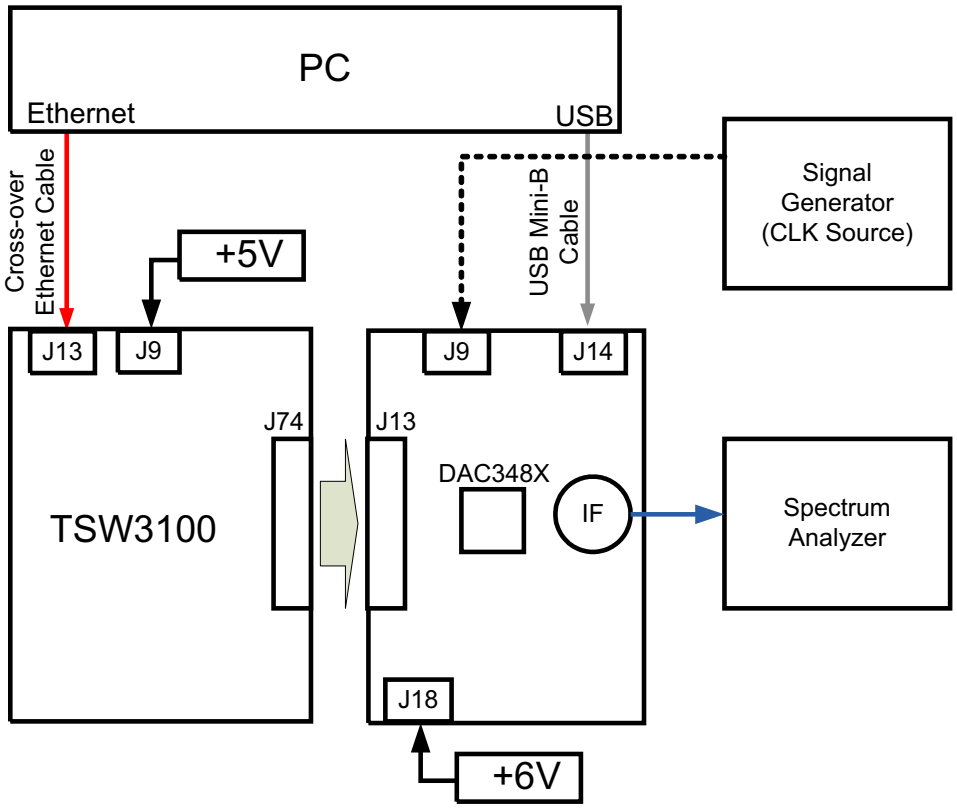

Figure 16. Test Set-up Block Diagram for TSW3100

4.3 Test Set-up Connection

- TSW3100 Pattern Generator
  1. Connect 5V power supply to J9, *5V_IN* jack of the TSW3100 EVM.
  2. Connect the PC's Ethernet port to J13, *Ethernet* port of the TSW3100. The cable should be a standard cross-over Cat5e Ethernet cable.
- DAC348x EVM
  1. Connect J13 connector of DAC348x EVM to J74 connector of TSW3100EVM.
  2. See the Test Setup Connection section.

4.4 DAC348x Example Setup Procedure

See the DAC348x Example Setup Procedure section.

4.5 TSW3100 Example Setup Procedure

Reference the TSW3100 User's Guide (SLWU079) for more detailed explanations of the TSW3100 set-up and operation. This document assumes the TSW3100 software is installed and functioning properly. *The DAC348x needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).*

CommsSignalPattern Setup from Default Configuration (WCDMA)

- Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (i.e. **1228.8 / 4/ 3.84 = 80**)
- Enter desired Offset Frequency (i.e. 30 MHz) for each desired carrier
- Select the **16b QDAC** output button for DAC3484 (see Figure 17) or **LVDS** output button for DAC3482, DAC34H84, and DAC34SH84 (see Figure 18).

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- Check the “LOAD and Run” box
- Press the green“Create” button
- **Toggle the SIF SYNC button of the DAC348x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**
- Verify the spectrum using the Spectrum Analyzer at the four IF outputs of the DAC348x EVM (J7, J6, J3, and J2).
  - For the DAC3482 EVM, the IF outputs are at the J6 and J3 SMA connector
- The expect results are shown in Figure 13 (NCO enabled at 30MHz) and Figure 14 (NCO disabled).

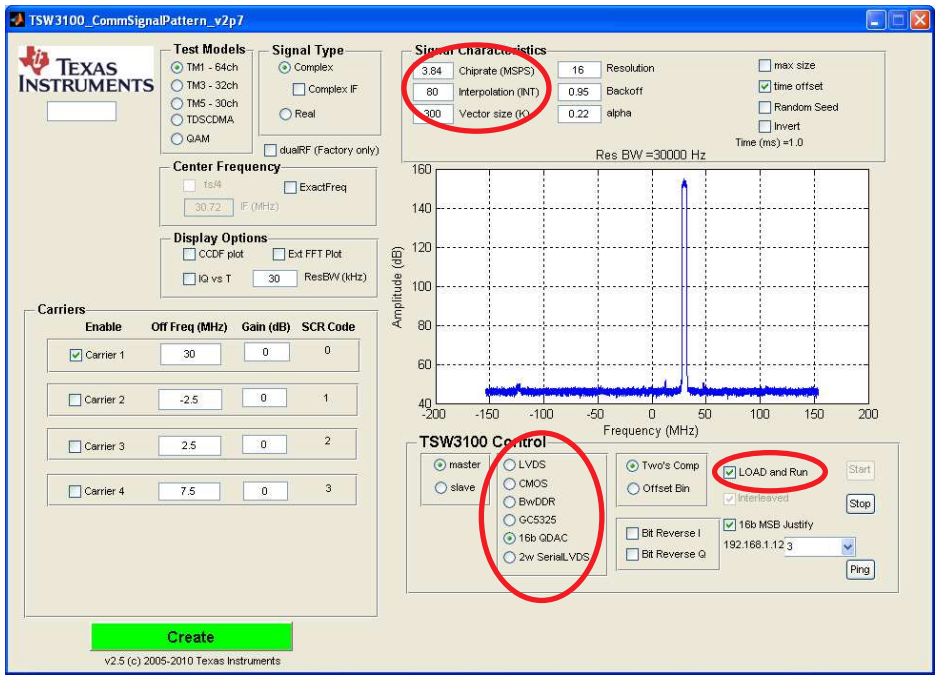

Figure 17. TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3484

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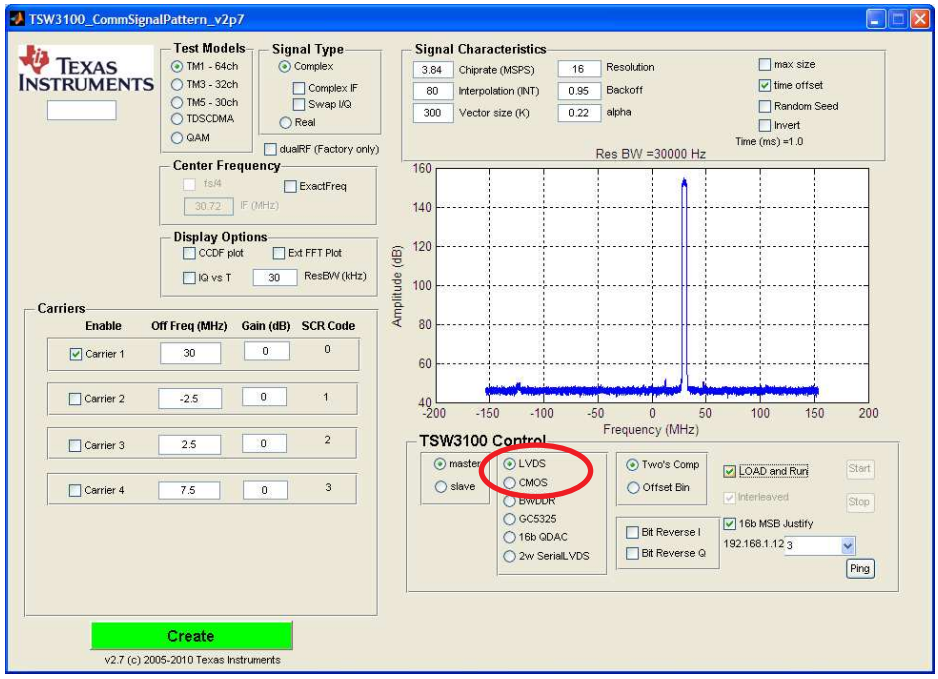

Figure 18. TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3482, DAC34H84, and DAC34SH84

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5 References

5.1 Related Products From Texas Instruments

Dual-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC3482 (SLAS748)

Quad-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC3484 (SLAS749)

Quad-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC34H84 (SLAS751)

Quad-Channel, 16-Bit, 1.5 GSPS Digital-to-Analog Converter (DAC) , DAC34SH84 (SLAS808)

Five/Ten Output Clock Generator/Jitter Cleaner With Integrated Dual VCO, CDCE62005 (SCAS862)

5.2 Related Tools From Texas Instruments

TSW1400 High Speed Data Capture/Pattern Generator Card (SLWU079)

TSW3100 High Speed Digital Pattern Generator (SLUU101)

FMC-DAC-ADAPTER Physical Design Database Rev D Board (SLOR102)

DAC34H84EVM Design Package board rev C (SLAC518)

DAC348x EVM Software (SLAC483)

High Speed Data Converter Pro software (SLWC107)

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Caution

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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REGULATORY COMPLIANCE INFORMATION (continued)

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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